AMENDMENTS TO THE CLAIMS:

1-13. (Cancelled)

14. (Original) A semiconductor device comprising a MOS transistor with a plurality of gate electrodes,

wherein the gate electrodes are formed on a semiconductor substrate having a silicon layer at least in the surface thereof,

the MOS transistor has a gate length of 0.15 μm or smaller and is formed in an element region surrounded with an isolation insulating film,

each of the gate electrodes is arranged between the other gate electrodes or between one of the other electrodes and a dummy pattern with a space left from each side thereof,

sidewalls are provided on side walls of each of the gate electrodes and on side walls of another said gate electrode,

a first silicide layer is formed in the upper portion of the gate electrode,

a second silicide layer is formed in a portion of the semiconductor substrate surface which is located in part of the element region between the gate electrode and at least one of another gate electrode and the dummy pattern, and

the first silicide layer has a greater thickness than the second silicide layer.

15. (Currently amended) The device of claim 14, wherein the dummy pattern is a dummy gate electrode which is an electrode pattern having the shape of a gate electrode, ~~side walls of the dummy pattern are provided with sidewalls,~~ and the dummy pattern is an electrode which is not electrically connected to a semiconductor integrated circuit of the semiconductor device.

16. (Original) The device of claim 14, wherein the dummy pattern is made of insulating material.

17. (Currently amended) The device of claim 14, wherein the dummy pattern is either a pattern made of ~~insulating material or~~ a dummy gate electrode which is an electrode pattern having the shape of a gate electrode with side walls of the dummy pattern provided with sidewalls and is not electrically connected to a semiconductor integrated circuit of the semiconductor device.

18. (Currently amended) The device of claim 16 ~~or 17~~, wherein the pattern made of insulating material is formed on the isolation insulating film.

19-24. (Cancelled)

25. (New) The device of claim 14, wherein dummy patterns are arranged on both sides of a group of the plurality of gate electrodes with a space left between each other,

one of the dummy patterns is a dummy gate electrode which is an electrode pattern having the shape of a gate electrode, and the other dummy pattern is a pattern made of insulating material.